WEST Search History

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DATE: Thursday, November 04, 2004

Hide?	Set Name	Query	Hit Count
		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L21	L20 and l19 and l18	1
☐	L20	(high bandwidth or highbandwidth or high-bandwidth) l4	1
☐	L19	(dynamic random access memory or DRAM) cache memories	156
☐	L18	multiprocessor chip	52
☐	L17	l4 same l15	1
☐	L16	l5 same L15	12
☐	L15	programmable l5	12
☐	L14	progammable l5	0
☐	L13	l3 same L12	2
☐	L12	l5 same l2	144
☐	L11	l5 same l4 same l3	1
☐	L10	l3 and l5 and l4 and l2	3
☐	L9	L6 and l4 and l2	1
☐	L8	L6 and l5 and l2	2
☐	L7	L6 and l5 and l2 and l1	2
☐	L6	l3 same L5	43
☐	L5	selector circuit	14076
☐	L4	signal bus	20272
☐	L3	cache memories	35578
☐	L2	redundant element or redundancies	84271
☐	L1	integrated circuit or IC	1439188

END OF SEARCH HISTORY